Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **A1**
2. **B1**
3. **Y1**
4. **Y2**
5. **A2**
6. **B2**
7. **VSS**
8. **A3**
9. **B3**
10. **Y3**
11. **Y4**
12. **A4**
13. **B4**
14. **VDD**

**.061”**

**.044”**

**12 11 10 9**

**13**

**14**

**1**

**8**

**7**

**6**

**2 3 4 5**

**MASK**

**REF**

**409320**

****

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD or FLOAT**

**Mask Ref: 4093**

**APPROVED BY: DK DIE SIZE .044” X .061” DATE: 8/17/21**

**MFG: SILICON SUPPLY THICKNESS .014” P/N: CD4093B**

**DG 10.1.2**

#### Rev B, 7/19/02